Study of the Effect of the C_{max}/C_{min} Ratio on the Performance of Back-to-Back Barrier-N-N (bbBNN) Varactor Frequency Multipliers

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***Abstract*— The effect of the C_{max}/C_{min} ratio on the performance of planar back-to-back Barrier-N-N$^+$ (bbBNN) frequency multipliers is studied. A simplified physical model of the device is used to relate the electrical characteristics to the material and the structural parameters. Multiplication efficiency is evaluated using a large signal analysis approach. Results indicate that if the optimum device size for a given frequency is used, a high C_{max}/C_{min} ratio results in high efficiency.**

I. Introduction

IN ORDER to improve the ruggedness of frequency multipliers for spaceborne local oscillator applications, planar varactor devices are being developed to replace whisker contacted devices. One candidate is the planar back-to-back Barrier-N-N- (bbBNN) varactor. It is a modification of the Barrier-Instrinsic-N$^+$ (BIN) varactor [1], providing a lower series resistance. It exhibits a very sharp capacitance versus voltage characteristic, resulting in efficient harmonic generation at small input power levels. It has symmetric C-V and anti-symmetric I-V characteristics. Symmetric impedance nonlinearities centered at zero bias will generate only odd harmonics, thereby simplifying the mount design.

A conceptual diagram of the bbBNN varactor is shown in Fig. 1. The layer thicknesses, doping densities, and compositions can be adjusted for optimum performance. The operation of the device as a varactor is described in the references [2], [3].

Previous studies on bbBNN and single barrier varactors [3,4] draw different conclusions on the impact of the C_{max}/C_{min} ratio on multiplier efficiency. In one case, the efficiency increased with C_{max}/C_{min} ratio [3], while in the other, it reached a maximum and then decreased [4]. In this paper, we study the effect of C_{max}/C_{min} ratio for two cases: 1) when C_{max} is held constant and 2) when C_{min} is held constant. Physically realizable device characteristics obtained from a simplified device model are used in a large signal analysis program to determine the RF performance.

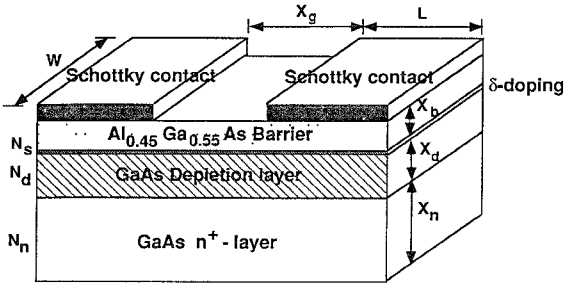

Fig. 1 Schematic diagram of a back-to-back BNN varactor.

II. Physical Device Modeling

We have theoretically designed several physically realizable devices having different C_{max}/C_{min} ratios. These devices are summarized in Table I, which includes device dimensions (illustrated in Fig. 1) and doping parameters as well as the series resistance, the breakdown voltage, and the dynamic cutoff frequency. To calculate device parameters, the depletion approximation was used. In addition, the three-dimensionality inherent in the back-to-back varactor was ignored. This assumption, neglecting fringing and parasitic capacitances, results in a lower minimum capacitance than is observed in real varactors.

Table I(a, b) show characteristics for 8μm^2 area devices with 2-μm-wide Schottky contacts across 4-μm–wide mesas and 2-μm separation between contacts. These dimensions are typical for those used in a 67 to 200-GHz tripler [5]. Table I(c, d) show characteristics for 4-μm^2 area devices with 1-μm-wide Schottky contacts. To assess the impact of the capacitance ratio C_{max}/C_{min} on efficiency, several devices for each area are considered. In Table I(a), C_{max} is constant at 30 fF, while the ratio C_{max}/C_{min} is varied between 5 and 2. In Table I(b), C_{min} is constant at 7.5 fF, while C_{max} is adjusted to vary the ratio of C_{max}/C_{min}. In Table I (part c), C_{max} is constant at 15 fF, since the area is a factor of 2 smaller than the device in Table I(a). Similarly, in Table I(d), C_{min} is constant at 3.75 fF.

C_{max} is determined by the barrier thickness, X_b, and the device area. The ratio of C_{max}/C_{min} sets the depletion region thickness, X_d. The δ-doping, n_s, and depletion region doping,

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TABLE I
PHYSICAL bbBNN DEVICE MODELING. VOLTAGE NEEDED TO DEPLETE THE DRIFT REGION IS 2.32 V

(a) $C_{\max}$= 30 fF, device area =8μm^2, $W = 4$ μm, $L = 2$ μm, $X_g = 2$ μm

$\frac{C_{max}}{C_{min}}$	X_b (nm)	X_d (nm)	n_s (cm^-2)	N_d (cm^-3)	R_s (Ω)	V_bd (volts)	F_cd (GHz)
5	15.3	122.5	2.95×10^{12}	1.30×10^{17}	10.4	23.5	2040
4	15.3	92.0	6.00×10^{12}	1.33×10^{17}	9.6	24.5	1650
3	15.3	61.0	5.00×1^{12}	3.24×10^{17}	8.2	22.5	1290
2	15.3	31.0	5.00×10^{12}	9.46×10^{17}	7.7	7.4	696

(b) $C_{\min}$= 7.5 fF, device area = 8μm^2, $W = 4$ μm, $L = 2$ μm, $X_g = 2$ μm

$\frac{C_{max}}{C_{min}}$	X_b (nm)	X_d (nm)	n_s (cm^-2)	N_d (cm^-3)	R_s Ω)	V_bd (volts)	F_cd (GHz)
5	12.3	98.1	7.70×10^{12}	1.20×10^{17}	10.0	12.3	1700
4	15.3	92.0	6.00×10^{12}	1.33×10^{17}	9.6	14.5	1650
3	20.4	81.9	4.00×10^{12}	1.70×10^{17}	9.0	16.6	1570
2	30.6	61.5	2.53×10^{12}	2.37×10^{17}	8.4	16.9	1270

(c) $C_{\max}$= 15 fF, device area =4μm^2, $W = 4$ μm, $L = 1$ μm, $X_g = 2$ μm

$\frac{C_{max}}{C_{min}}$	X_b (nm)	X_d (nm)	n_s (cm^-2)	N_d (cm^-3)	R_s (Ω)	V_bd (volts)	F_cd (GHz)
5	15.3	122.5	2.95×10^{12}	1.30×10^{17}	12.0	23.5	3510
4	15.3	92.0	5.75×10^{12}	1.40×10^{17}	10.4	14.8	3060
3	15.3	61.5	7.00×10^{12}	2.10×10^{17}	8.3	9.9	2580
2	15.3	30.7	7.85×10^{12}	5.00×10^{17}	6.9	6.2	1540

(d) $C_{\min}$= 3.75 fF, device area =4μm^2, $W = 4$ μm, $L = 1$ μm, $X_g = 2$ μm

$\frac{C_{max}}{C_{min}}$	X_b (nm)	X_d (nm)	n_s (cm^-2)	N_d (cm^-3)	R_s (Ω)	V_bd (volts)	F_cd (GHz)
5	12.3	98.1	7.70×10^{12}	1.20×10^{17}	11.3	12.3	3004
4	15.3	92.0	6.00×10^{12}	1.33×10^{17}	10.6	14.5	3004
3	20.4	81.9	4.50×10^{12}	1.50×10^{17}	9.7	16.0	2910
2	30.7	61.5	3.48×10^{12}	1.60×10^{17}	8.8	16.0	2420

N_d, were adjusted so that the voltage necessary to completely deplete the depletion region is held constant at 2.32 V.

The device series resistance R_s is given by,

$$R_s = R_d + R_n + R_p \tag{1}$$

where R_d is the resistance of the depletion region, R_n is the resistance of the n^+ region and R_p is the parasitic metal resistance. The depletion region resistance R_d and the resistance due to the n^+ region, R_n are given by,

$$R_d = (1.5 \cdot x_d)/(L \cdot W \cdot q \cdot \mu_d \cdot N_d), \tag{2}$$

and

$$R_n = (L + X_g)/(W \cdot X_n \cdot q \cdot \mu_n \cdot N_n), \tag{3}$$

where X_d and X_n are the thicknesses, N_d and N_n are the doping densities, and μ_d and μ_n are the mobilities of the depletion region and the n^+ region, respectively. L is the length of the metal pad, W is the width of the metal pad, and X_g is the gap between the metal pads (Fig. 1). The factor 1.5 in R_d is used to approximate an average resistance over one cycle since depletion region width is a function of applied voltage and varies throughout the pump cycle. The mobilities of the depletion and n^+ regions are assumed to be 0.4 and 0.2 m^2/V-s, respectively. The parasitic metal resistance R_p due to the Ti/Pt/Au fingers was calculated to be 0.67 Ω and 1.3-Ω, for 8-μm^2 and 4-μm^2 device areas, respectively. The series resistance values of 7–12 Ω are in reasonable agreement with measurements [5]. The resistance of the n^+ region is the dominating part in the series resistance values.

The breakdown voltage V_{bd}, modeled here, is due to Fowler-Nordheim tunneling [2]. Devices made in the laboratory have always shown lower breakdown voltages than the modeling indicates. This may be due to an avalanche mechanism.

The dynamic cut-off frequency of the device was determined by the formula

$$f_{cd} = [1/(2 \cdot \pi \cdot R_s \cdot C_{\min})] \cdot [1 - (C_{\min}/C_{\max})] \tag{4}$$

where R^s is the series resistance modeled at zero bias.

III. LARGE SIGNAL ANALYSIS

The effect of $C_{\max}/C_{\min}$ on bbBNN varactor tripler efficiency from 67 to 200 GHz was evaluated for the devices in Table I, using a modified version of the nonlinear program by Siegel *et al.* [6]. Embedding network impedances at the input and output frequencies were optimized. Other harmonic embedding impedances were assumed to be open circuited. The effect of velocity saturation [7] have not been included and will reduce the performance for high pump power and high frequencies.

The results are shown in Fig. 2, where the tripling efficiency is plotted as a function of input power parameterized by the $C_{\max}/C_{\min}$ ratio. Fig. 2(a) and (b) show the result for bbBNN with areas of 8-μm^2, Fig. 2(c) and (d) show the result for 4-μm^2 device area. In Fig. 2(a) and (c), the maximum capacitance has been held constant, while in Fig. 2(c) and (d), the minimum capacitance is constant.

As can be seen in Fig.2, the peak efficiency is highest for the device with highest f_{cd}, the dynamic cut-off frequency of the device. The pump power at which the peak efficiency is obtained depends primarily on $C_{\max}$ since the voltage to completely deplete the depletion region is fixed for all cases presented here. Hence, the 8-μm^2 device [Fig. 2(a) and (b)] requires more pump power for peak efficiency than the 4-μm^2 device [Fig. 2(c) and (d)]. In the case where $C_{\max}$ is fixed [Fig. 2(a) and (c)], the pump power for peak efficiency is roughly constant. However, in the case when $C_{\min}$ is fixed [Fig. 2(b) and (d)] and $C_{\max}$ varies, the pump power for peak efficiency increases with $C_{\max}$ and hence with the $C_{\max}/C_{\min}$ ratio.

IV. CONCLUSION

From the above simulations, the previous discrepancy on the impact of $C_{\max}/C_{\min}$ ratio can be understood. In one case [3], the $C_{\max}$ was fixed, whereas in the other case [4], $C_{\min}$ was fixed. When $C_{\max}$ is fixed, the efficiency is always

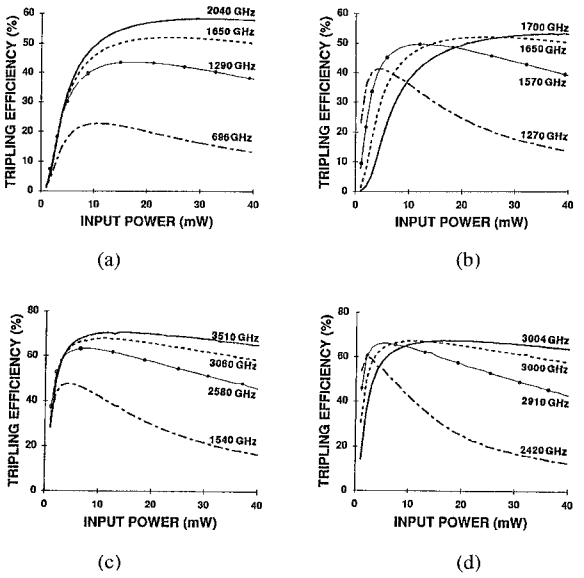

Fig. 2. Tripling efficiency versus input power plot for 67 to 200-GHz tripler parameterized by $C_{\max}/C_{\min}$ and dynamic cut-off frequency of the device. (a) $C_{\max} = 30$ fF, variation of $C_{\min}$ (device area = 8 μm^2). (b) $C_{\min} = 7.5$ fF, variation of $C_{\max}$ (device area = 8 μm^2). (c) $C_{\max} = 15$ fF, variation of $C_{\min}$ (device area = 4 μm^2). (d) $C_{\min} = 3.75$ fF, variation of $C_{\max}$ (device area = 4 μm^2). ——— $C_{\max}/C_{\min} = 5$, - - - - - - - $C_{\max}/C_{\min} = 4$, ———o———o———o— $C_{\max}/C_{\min} = 3$, ——— — ——— — ——— $C_{\max}/C_{\min} = 2$.

improved with high $C_{\max}/C_{\min}$. For the fixed $C_{\min}$ case, if a low input power (for the cases studied here below about 10 mW) is also assumed, the efficiency would peak for an intermediate $C_{\max}/C_{\min}$ ratio. This is especially true if the diode area is large. But if a higher input power (15 mW or more) is used with the optimum device size for the given frequency, the highest possible $C_{\max}/C_{\min}$ ratio results in maximum efficiency. Thus a "rule of thumb" is that the highest dynamic cut-off frequency, f_{cd} and the highest $C_{\max}/C_{\min}$ gives the best multiplication efficiency.

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